Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising:

an initiator interface;

a target interface;

a storage buffer circuit having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and

a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising:

a write pointer register connected to the storage buffer circuit and clocked at the storage buffer input clock rate to control the storage location at which data is written into the storage buffer circuit;

a read pointer register connected to the storage buffer circuit and clocked at the storage buffer output clock rate to control the storage location from which data is read from the storage buffer circuit;

a first retiming circuit coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate;

a second retiming circuit coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate;

a first comparator connected to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output dependent thereon;

a second comparator connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output dependent thereon;

write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator; and

read control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator;

and wherein the write control logic in the storage buffer control circuit is adapted to control the write pointer register such that data, making up a data packet, received at the data input of the associated storage buffer circuit is written into successive storage locations of the storage buffer circuit as the data is received so long as the storage locations are not all full, and the read control logic in the storage buffer control circuit is adapted to control the read pointer register such that data in the storage locations is only read after a predetermined time delay, the time delay being such that when all the said storage locations are read from successively a complete data packet without gaps is applied to the data output of the storage buffer circuit.

2. (Original) A bridge circuit according to claim 1, wherein the predetermined time delay is a predetermined number of clock cycles of either buffer input or output clock.

3. (Canceled)

4. (Original) A bridge circuit according to claim 1, in which the read control logic also causes all the full storage locations to be read from on receipt of an end-of-packet signal.

5. (Original) A bridge circuit according to claim 1, in which the comparators provide outputs indicating at least when the storage buffer circuit is full and is empty.

6. (Original) A bridge circuit according to claim 1, in which the maximum number of storage locations to be made available simultaneously is predetermined, the write control logic is adapted to determine when the storage buffer circuit is full.

7. (Original) A bridge circuit according to claim 1, in which each retiming circuit includes a Gray coder clocked at the input clock rate of the retiming circuit.

8. (Original) A bridge circuit according to claim 1, in which each retiming circuit is adapted to provide a plurality of possible degrees of retiming, and including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming.

9. (Original) A bridge circuit according to claim 8, in which each retiming circuit includes two retiming elements connected in cascade, and a selector, the selector being connected to receive the input to the retiming elements and the output of each of the retiming elements and to select one of its inputs as the output in dependence upon the mode signal.

10. (Original) A bridge circuit according to claim 8, in which the mode signal is adapted to be changed during operation of the bridge circuit.

11. (Original) A bridge circuit according to claim 10, further comprising a strobe retiming circuit connected to receive a strobe signal and retime it relative to the initiator clock, an edge detector for detecting an edge in the strobe signal, a mode signal timing circuit for timing the mode signal relative to the output of the edge detector, and a mode signal change detection circuit connected to the output of the mode signal timing circuit to detect a change in the mode signal and to provide a change signal in response thereto.

12. (Original) A bridge circuit according to claim 1, further comprising a bypass for the storage buffer circuit, and a selector for selecting either the storage buffer circuit or the bypass in accordance with a mode signal received at an input.

13. (Currently Amended) A bridge circuit according to claim 1, further comprising a second storage buffer circuit having a data input connected to the target interface and a data output connected to the initiator interface ~~and a data output connected to the initiator interface~~ and having a plurality of storage locations, and a second storage buffer control circuit similar to the first-mentioned storage buffer control circuit connected to control the second storage buffer circuit.

14. (Original) A semiconductor integrated circuit comprising at least one bridge circuit in accordance with claim 1.

15. (Previously Presented) A bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising:

an initiator interface;

a target interface;

a storage buffer circuit having a data input connected to the initiator interface and a data output connected to the target interface, and having a plurality of storage locations; and

a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising:

a write pointer register connected to the storage buffer circuit and clocked at the storage buffer input clock rate to control the storage location at which data is written into the storage buffer circuit;

a read pointer register connected to the storage buffer circuit and clocked at the storage buffer output clock rate to control the storage location from which data is read from the storage buffer circuit;

a first retiming circuit coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate comprising one or more retiming buffers and a selector connected to receive inputs from each of the retiming buffers;

a second retiming circuit coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate comprising one or more retiming buffers and a selector connected to receive inputs from each of the retiming buffers;

a first comparator connected to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output dependent thereon;

a second comparator connected to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output dependent thereon;

write control logic connected to receive the output of the first comparator and connected to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator; and

read control logic connected to receive the output of the second comparator and connected to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator;

wherein the storage buffer control circuit is adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators and wherein, when one or more retiming buffers are in the path from the read or write pointer registers to the comparators, the read control logic is adapted to control the read pointer register such that data in the storage locations is only read after a predetermined time delay, the time delay being such that all the storage locations are read from successively and a complete data packet without gaps is provided to the data output.

16. (Original) A bridge circuit according to claim 15, in which each retiming circuit is adapted to provide a plurality of possible degrees of retiming, and including a mode

signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming.

17. (Original) A bridge circuit according to claim 15, in which each retiming circuit includes two retiming elements connected in cascade, and a selector, the selector being connected to receive the input to the retiming elements and the output of each of the retiming elements and to select one of its inputs as the output in dependence upon the mode signal.

18. (Original) A bridge circuit according to claim 15, in which the mode signal is adapted to be changed during operation of the bridge circuit.

19. (Original) A bridge circuit according to claim 15, wherein each retiming buffer comprises a D-type flip-flop for each bit in the pointer register output, whereby zero or more D-type flip-flops are selectively chosen for retiming.

20. (Original) A bridge circuit according to claim 15, wherein selectively 0, 1 or 2 D-type flip-flops are selected for retiming.

21. (New) A bridge circuit for use in retiming in a semiconductor integrated circuit, the bridge circuit comprising:

an initiator interface;

a target interface;

a storage buffer circuit having a data input coupled to the initiator interface and a data output coupled to the target interface, and having a plurality of storage locations; and

a storage buffer control circuit associated with the storage buffer circuit; the storage buffer control circuit comprising:

a write pointer register coupled to the storage buffer circuit and clocked at the storage buffer input clock rate, the write pointer register configurable to hold a first identifier of a storage location at which data is written into the storage buffer circuit;

a read pointer register coupled to the storage buffer circuit and clocked at the storage buffer output clock rate, the read pointer register configurable to hold a second identifier, different from the first identifier, of a storage location from which data is read from the storage buffer circuit;

a first retiming circuit coupled to the output of the read pointer register to retime the output of the read pointer register with reference to the storage buffer input clock rate;

a second retiming circuit coupled to the output of the write pointer register to retime the output of the write pointer register with reference to the storage buffer output clock rate;

a first comparator coupled to receive and compare the outputs of the write pointer register and the first retiming circuit and to provide an output dependent thereon;

a second comparator coupled to receive and compare the outputs of the read pointer register and the second retiming circuit and to provide an output dependent thereon;

write control logic coupled to receive the output of the first comparator and coupled to the write pointer register to increment the count held in the write pointer register in dependence upon the output of the first comparator; and

read control logic coupled to receive the output of the second comparator and coupled to the read pointer register to increment the count held in the read pointer register in dependence upon the output of the second comparator;

and wherein the write control logic in the storage buffer control circuit is adapted to control the write pointer register such that data, making up a data packet, received at the data input of the associated storage buffer circuit is written into successive storage locations of the storage buffer circuit as the data is received so long as the storage locations are not all full, and the read control logic in the storage buffer control circuit is adapted to control the read pointer register such that data in the storage locations is only read after a predetermined time delay, the time delay being such that when all the said storage locations are read from successively a complete data packet without gaps is applied to the data output of the storage buffer circuit.